19-1436; Rev 2; 3/02

EVALUATION KIT MANUAL AVAILABLE

3A, Low-Voltage, Step-Down Regulator with Synchronous Rectification and Internal Switches

General Description

The MAX1623 switch-mode buck regulator with synchronous rectification provides local CPU and bus-termination power in notebook and desktop computers. An internal 55mΩ (typ), 3A PMOS power switch and 60mΩ (typ), 3A NMOS synchronous-rectifier switch deliver continuous load currents up to 3A from a 5V supply with 95% typical efficiency. Output accuracy is ±1%, including line and load regulation.

The MAX1623 features constant-off-time, current-mode pulse-width-modulation (PWM) control with switching frequencies as high as 350kHz. An external resistor at the TOFF pin sets the off-time, allowing optimum design flexibility in terms of switching frequency, output switching noise, and inductor size. This device is available in a space-saving 20-pin SSOP package.

Applications

5V to 3.3V Conversion

Notebook Computer CPU I/O Supply

Desktop Computer Bus-Termination Supply

CPU Daughter Card Supply

DSP Supply

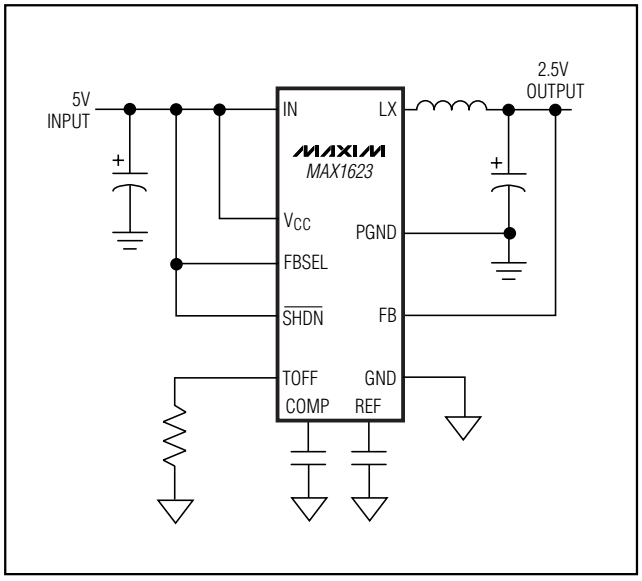
Features

- ♦ **±1% Output Accuracy, Including Line and Load Regulation**
- ♦ **94% Efficiency**
- ♦ **Internal Switches**
  55mΩ PMOS Power Switch
  60mΩ NMOS Synchronous-Rectifier Switch
- ♦ **Guaranteed 3A Load Capability**
- ♦ **Minimal External Components**
- ♦ **Pin-Selectable Fixed 3.3V, 2.5V, or Adjustable (1.1V to 3.8V) Output Voltage**
- ♦ **4.5V to 5.5V Input Voltage Range**
- ♦ **400µA (typ) Supply Current**
- ♦ **<1µA Shutdown Supply Current**
- ♦ **Constant-Off-Time PWM Operation**
- ♦ **Switching Frequencies Up to 350kHz**
- ♦ **Idle Mode™ Operation at Light Loads**
- ♦ **Thermal Shutdown Protection**
- ♦ **Available in 20-Pin SSOP**

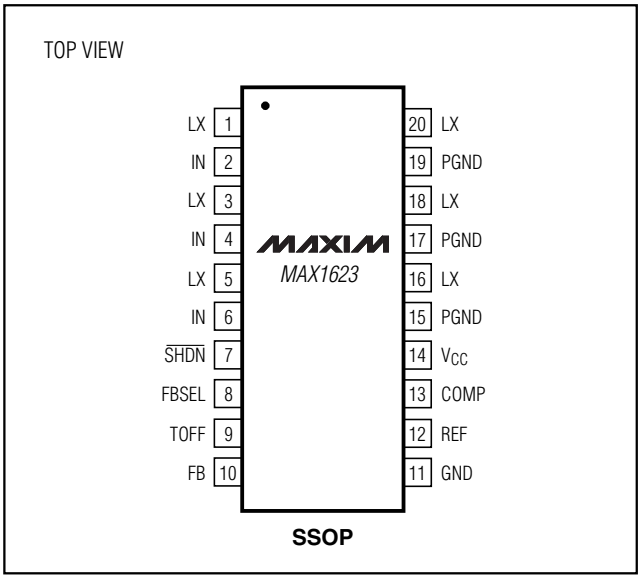
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1623EAP	-40°C to +85°C	20 SSOP

Typical Operating Circuit



Pin Configuration



Idle Mode is a trademark of Maxim Integrated Products.

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

3A, Low-Voltage, Step-Down Regulator with Synchronous Rectification and Internal Switches

ABSOLUTE MAXIMUM RATINGS

IN to PGND .....0V to 6V
V_{CC} to GND .....-0.3V to 6V
PGND to GND.....±0.5V
IN to V_{CC}.....±0.5V
LX Current (Note 1).....±5.5A
$\overline{SHDN}$ to GND.....-0.3V to 6V
REF, FBSEL, COMP, FB, TOFF to GND .....-0.3V to (V_{CC} + 0.3V)
REF Short to GND .....Continuous
Continuous Power Dissipation (T_A = +70°C) (with part mounted on 1 sq. inch of one ounce copper)
20-Pin SSOP (derate 22mW/°C above +70°C) 1.3W
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: LX has internal clamp diodes to PGND and IN. Applications that forward bias these diodes should take care not to exceed the IC's package power dissipation limits.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = V_{CC} = 5V, FBSEL unconnected, R_{TOFF} = 110kΩ, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range			4.5		5.5	V
Output Voltage	V_{IN} = 4.5V to 5.5V, I_{LOAD} = 0 to 3A	FBSEL = unconnected	3.296	3.330	3.366	V
		FBSEL = V_{CC}	2.49	2.525	2.550	
		FBSEL = GND or REF	1.089	1.100	1.110	
Output Adjustment Range	FBSEL = GND or REF (Note 2)		V_{REF}		3.80	V
Reference Output Voltage	I_{REF} = 0		1.089	1.100	1.110	V
Reference Load Regulation	I_{REF} = -1µA to 10µA				1	mV
Current-Limit Threshold			3.65		4.65	A
RMS LX Output Current					3.65	A
PMOS Switch On-Resistance	V_{IN} = 4.5V			55	100	mΩ
NMOS Switch On-Resistance	V_{IN} = 4.5V			60	100	mΩ
Maximum Switching Frequency	I_{LOAD} ≥ 1.5A (Note 2)				350	kHz
Idle Mode Threshold (Note 3)			1	1.25	1.5	A
No-Load Supply Current	Does not include switching losses			400	525	µA
Shutdown Supply Current	$\overline{SHDN}$ = GND			0.5	10	µA
LX Leakage Current	V_{IN} = 5.5V, V_{LX} = 5.5V or 0				±20	µA
Thermal Shutdown Threshold				145		°C
Undervoltage Lockout Threshold	V_{CC} falling, 100mV hysteresis		4.1	4.2	4.3	V
FB Input Bias Current	FBSEL = GND, adjustable output mode, V_{FB} = 1.2V		-25		25	nA
Error-Amplifier Gain Bandwidth	(Note 2)		500			kHz
Off-Time Adjustment Range			0.5		4	µs
Off-Time Default Period			0.85	1.00	1.15	µs
AC Output Load Regulation	FBSEL = GND			1		%
	FBSEL = REF			2		
$\overline{SHDN}$ Input Current	$\overline{SHDN}$ = GND or V_{CC}		-1	0.03	1	µA
$\overline{SHDN}$ Input Low Voltage					0.8	V
$\overline{SHDN}$ Input High Voltage			2			V

ELECTRICAL CHARACTERISTICS

(V_{IN} = V_{CC} = 5V, FBSEL unconnected, R_{TOFF} = 110kΩ, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range			4.5		5.5	V
Output Voltage	V_{IN} = 4.5V to 5.5V, I_{LOAD} = 0 to 3A	FBSEL = unconnected	3.234		3.366	V
		FBSEL = V_{CC}	2.450		2.550	
		FBSEL = GND or REF	1.075		1.110	
Output Adjustment Range	FBSEL = GND or REF (Note 2)		V_{REF}		3.8	V
Reference Output Voltage	I_{REF} = 0		1.075		1.110	V
Current-Limit Threshold			3.5		4.75	A
PMOS Switch On-Resistance	V_{IN} = 4.5V				0.1	Ω
NMOS Switch On-Resistance	V_{IN} = 4.5V				0.1	Ω
No-Load Supply Current	Does not include switching losses				600	µA
Shutdown Supply Current	$\overline{SHDN}$ = GND				10	µA
LX Leakage Current	V_{IN} = 5.5V, V_{LX} = 5.5V or 0		-20		20	µA
Undervoltage Lockout Threshold	V_{CC} falling, 100mV hysteresis		4.0		4.3	V
FB Input Bias Current	FBSEL = GND, adjustable output mode, V_{FB} = 1.2V		-50		50	nA
Off-Time Adjustment Range			0.55		4	µs
Off-Time Default Period			0.85		1.25	µs
$\overline{SHDN}$ Input Current	$\overline{SHDN}$ = GND or V_{CC}		-1		1	µA
$\overline{SHDN}$ Input Low Voltage					0.8	V
$\overline{SHDN}$ Input High Voltage			2.2			V

Note 2: Guaranteed by design, not production tested.

Note 3: Idle Mode threshold is defined as the transition point in the load-current range between Idle Mode and constant-off-time operation.

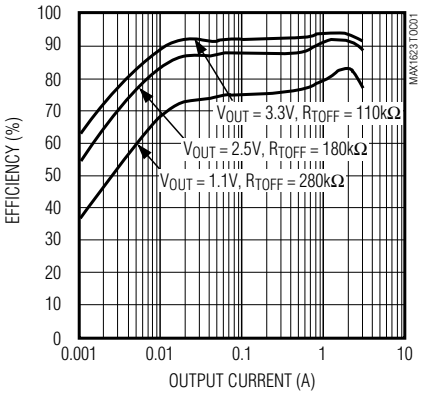
Note 4: Specifications to -40°C are guaranteed by design, not production tested.

3A, Low-Voltage, Step-Down Regulator with Synchronous Rectification and Internal Switches

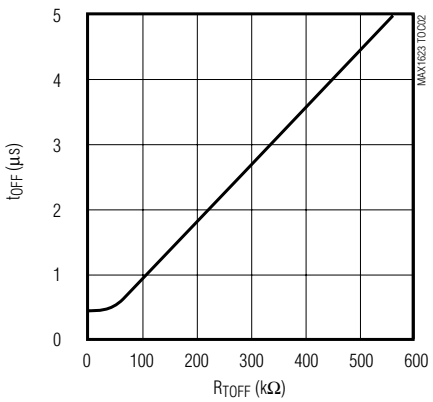
Typical Operating Characteristics

(Circuit of Figure 2, T_A = +25°C, unless otherwise noted.)

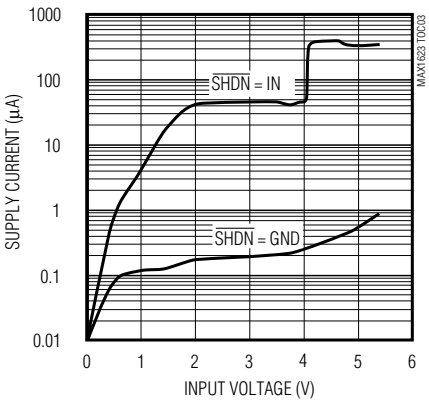
EFFICIENCY vs. OUTPUT CURRENT



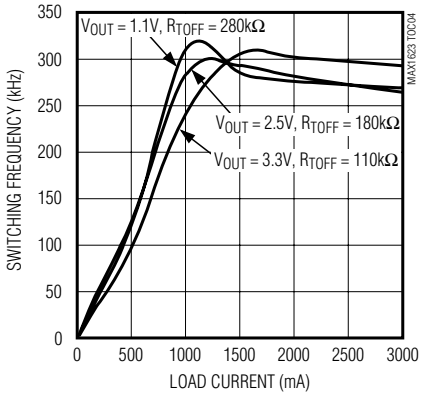
SWITCH OFF-TIME vs. OFF-TIME RESISTANCE



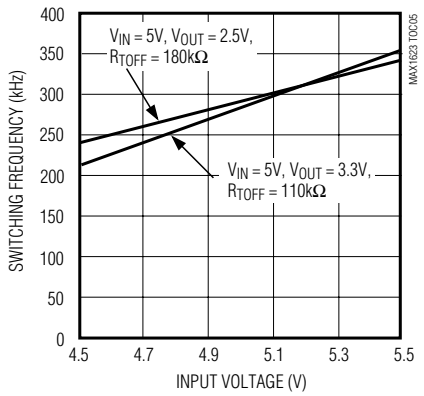
SUPPLY CURRENT vs. INPUT VOLTAGE



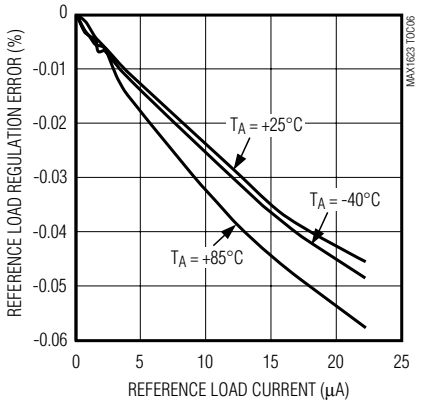
SWITCHING FREQUENCY vs. LOAD CURRENT



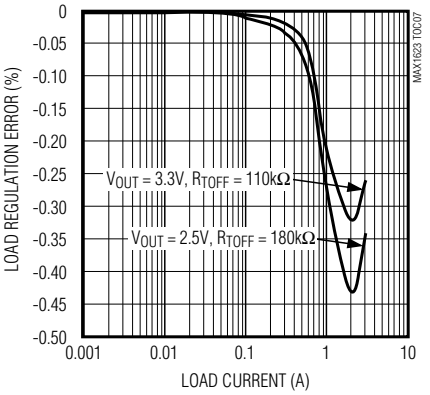
SWITCHING FREQUENCY vs. INPUT VOLTAGE



REFERENCE LOAD REGULATION ERROR vs. REFERENCE LOAD CURRENT



LOAD REGULATION ERROR vs. LOAD CURRENT

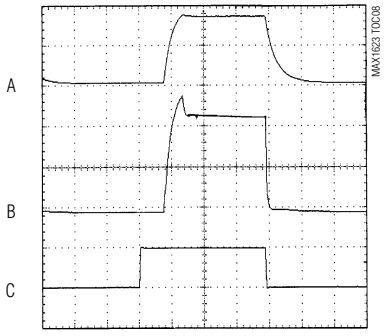


3A, Low-Voltage, Step-Down Regulator with Synchronous Rectification and Internal Switches

Typical Operating Characteristics (continued)

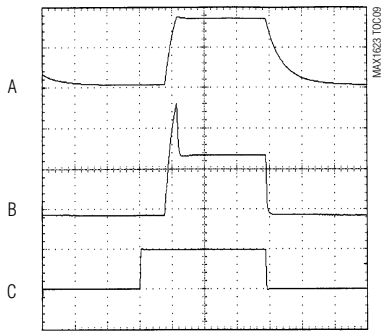
(Circuit of Figure 2, T_A = +25°C, unless otherwise noted.)

START-UP AND SHUTDOWN TRANSIENT



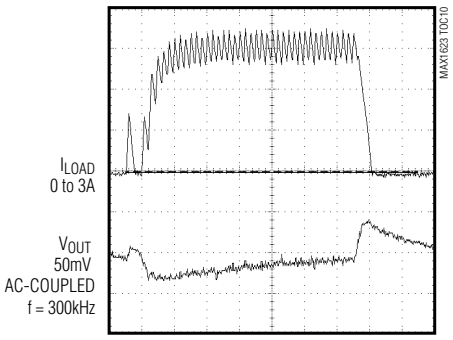
V_{IN} = 5V, V_{OUT} = 3.3V, I_{LOAD} = 3A,
WAVEFORM AVERAGED
A: V_{OUT}, 2V/div
B: I_{IN}, 1A/div
C: $V_{\overline{SHDN}}$, 5V/div

START-UP AND SHUTDOWN TRANSIENT

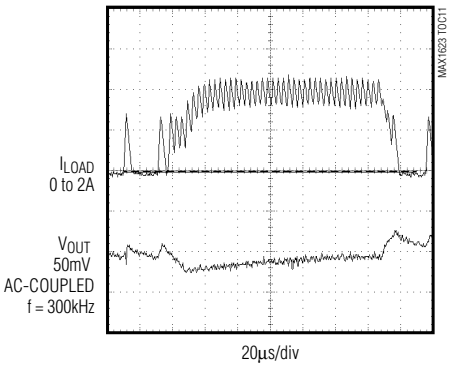


V_{IN} = 5V, V_{OUT} = 3.3V, I_{LOAD} = 2A,
WAVEFORM AVERAGED
A: V_{OUT}, 2V/div
B: I_{IN}, 1A/div
C: $V_{\overline{SHDN}}$, 5V/div

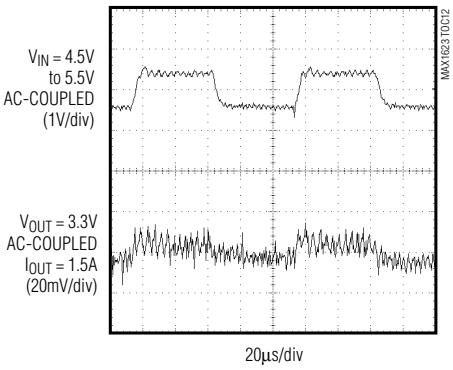
LOAD-TRANSIENT RESPONSE (FBSEL = REF)



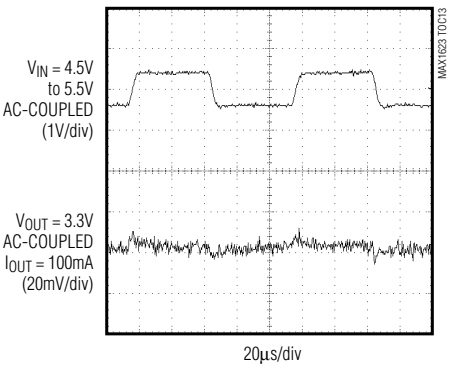
LOAD-TRANSIENT RESPONSE (FBSEL = REF)



LINE-TRANSIENT RESPONSE



LINE-TRANSIENT RESPONSE



3A, Low-Voltage, Step-Down Regulator with Synchronous Rectification and Internal Switches

Pin Description

PIN	NAME	FUNCTION
1, 3, 5, 16,18, 20	LX	Connection to the internal power switches.
2, 4, 6	IN	Power Input. Internally connected to the PMOS switch source. Connect to 5V.
7	$\overline{SHDN}$	Active-Low Shutdown Input. Connect to V_{CC} for normal operation.
8	FBSEL	Feedback Select Input. See Table 1.
9	TOFF	Off-Time Select Input. Connect a resistor from TOFF to GND to adjust the switch off-time, and therefore the frequency: $t_{OFF} = \frac{R_{TOFF}}{110k\Omega}$ (µs). See the *Typical Operating Characteristics*.
10	FB	Feedback input for both fixed-output and adjustable operating modes. Connect to the output directly for fixed-voltage operation or to a resistor-divider for adjustable operating modes.
11	GND	Analog Ground
12	REF	Reference Output. Bypass with a minimum 0.1µF capacitor to GND. See the *Internal Reference* section.
13	COMP	Integrator Capacitor Connection. Connect a 470pF (470pF to 2000pF range) capacitor to GND to set the typical integration time-constant. See the *Integrator Amplifier* section.
14	V_{CC}	Analog Supply-Voltage Input. Supplies internal analog circuitry. Connect to 5V. Bypass V_{CC} with 10Ω and 4.7µF (Figure 2).
15, 17, 19	PGND	Power Ground. Internally connected to the NMOS synchronous rectifier source.

General Description

The MAX1623 current-mode, PWM, DC-DC regulator is designed for 5V-input step-down applications. It features a 55mΩ (typ) PMOS switch and a 60mΩ (typ) NMOS synchronous-rectifier switch. Simple constant-off-time control allows switching frequencies up to 350kHz. Adjust the off-time with an external resistor R_{TOFF} to optimize performance trade-offs among efficiency, component size, output switching noise, and cost. Idle Mode operation enhances light-load efficiency by switching to a pulse-skipping mode that reduces transition and gate-charge losses. The power-switching circuit consists of the IC and an LC output filter. The output voltage is the average of the AC voltage at the switching node (LX). The MAX1623 regulates the output voltage by changing the PMOS switch on-time relative to the constant off-time, thereby adjusting the duty cycle.

The MAX1623 contains six major circuit blocks (Figure 1): a PWM comparator, a current-sense circuit, a PWM logic block, an internal feedback mux, an off-time control block, and a 1.1V precision reference. The input supply directly powers the internal blocks.

Modes of Operation

The load current determines the mode of operation: Idle Mode (load currents less than 0.625A) or PWM mode for inductor currents of 1.25A (which corresponds to load currents greater than 0.625A). The PWM current limit is continuously adjusted by the PWM comparator and can vary from 0A to the maximum current limit (4A). If the inductor current falls below the Idle Mode threshold (1.25A), skip mode takes over. Whenever the P-channel switch turns on, it stays on until the sensed current reaches the active current limit. The PWM current limit automatically adjusts with the PMOS switch duty cycle required to generate the desired output voltage. When the active current limit is met, the PMOS switch turns off for the programmed minimum off-time, and the N-channel synchronous rectifier turns on. The synchronous rectifier stays on until the P-channel switch turns back on or until the inductor current reaches zero. At the end of the off-time, the P-channel switch turns on again if the output voltage indicates that energy is required at the output.

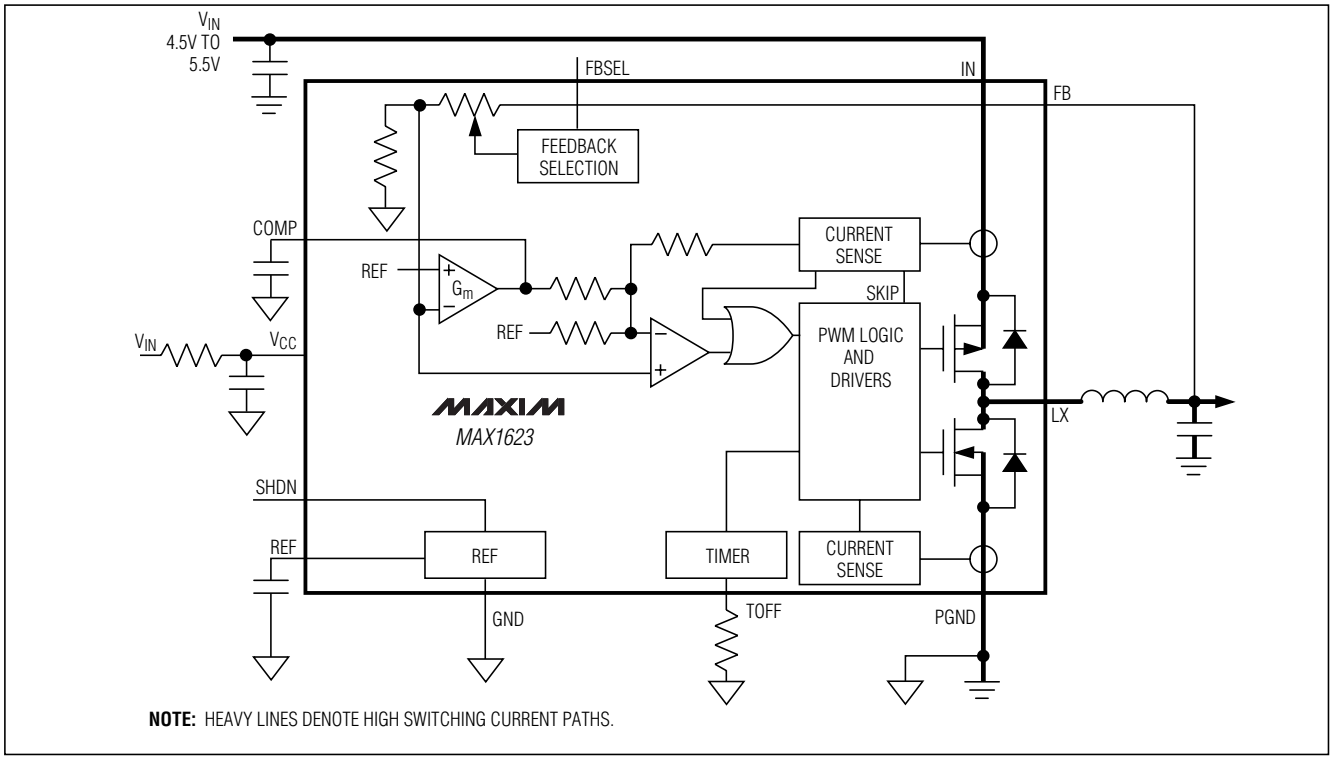


Figure 1. Functional Diagram

Idle Mode

At light loads, the device goes into skip mode (because the load current is below the skip threshold), and Idle Mode operation (1.25A current limit) begins. This allows both switches to remain off at the end of the off-time, skipping cycles to reduce switching losses. At lighter loads, the inductor current is discontinuous because the inductor current reaches zero. In Idle Mode, the operating frequency varies with output load current. There is no major shift in circuit behavior as the PWM limit falls below the skip limit. The effective off-time simply increases, resulting in a seamless transition between PWM mode and Idle Mode.

PWM Mode

PWM operation occurs whenever the load current is greater than the skip threshold. In this mode, the PWM comparator adjusts the current limit to the desired output current, so that the P-channel turns on at the end of each off-time.

Three signals are resistively summed at the input of the PWM comparator (Figure 1): an output voltage error signal relative to the reference voltage, an integrated output voltage error correction signal, and the sensed PMOS switch current. The integrated error signal is provided by a transconductance amplifier with an external capacitor at the COMP pin. This integrator provides high DC accuracy without the need for a high-gain error amplifier. Connecting a capacitor at COMP modifies the overall loop response (see the *Integrator Comparator* section).

Setting the Output Voltage

There are two preset output voltages (2.525V and 3.33V), or the output voltage can be adjusted from the reference voltage (nominally 1.1V) up to 3.8V. For a preset output voltage (Figure 2), connect FB to the output voltage, and connect FBSEL to V_{CC} (2.525V output) or leave it unconnected (3.33V output). For an adjustable output, connect FBSEL to GND or REF, and connect FB to the midpoint of a resistor divider between the output voltage and ground (Figure 3). Regulation is maintained when V_{FB} equals V_{REF}. Select R1 in the 10kΩ to 500kΩ range. R2 is given by:

$$R2 = (R1)(V_{OUT} / V_{REF} - 1)$$

where V_{REF} is typically 1.1V.

3A, Low-Voltage, Step-Down Regulator with Synchronous Rectification and Internal Switches

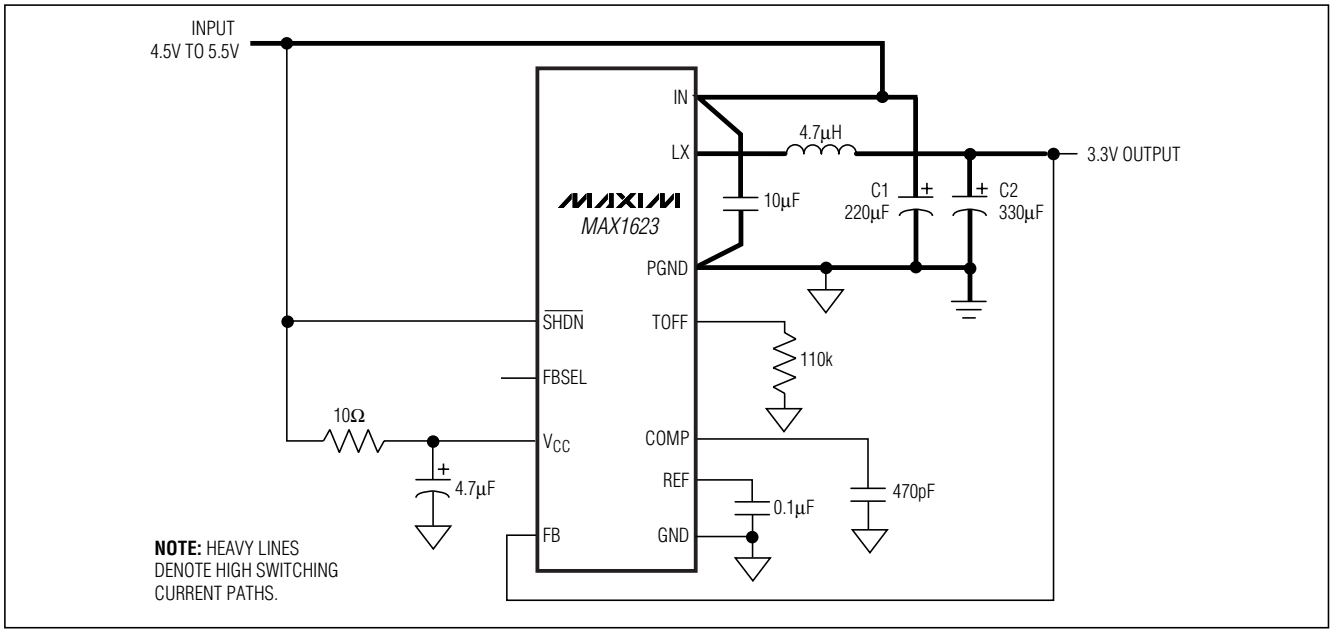


Figure 2. Standard 3.3V/3A Application Circuit

Setting the AC Loop Gain

The internal integrator amplifier effectively eliminates any long-term error within the time constant set by the G_m of the transconductance amplifier and the capacitor connected to COMP. However, there remains a short-term load-regulation error in response to load current changes. Proper FBSEL connection selects the relative level of current feedback to voltage feedback, which results in an AC load-regulation error of either 1% or 2% of the output voltage (Table 1). The 2% setting is automatically selected in preset output voltage mode (FBSEL connected to V_{CC} or unconnected). This gain setting minimizes the size and cost of the output filter capacitor required. For extremely tight specifications that cannot tolerate 2% short-term errors, connect FBSEL to ground (adjustable mode) for 1% AC load regulation (see the *Input and Output Filter Capacitors (C1, C2)* section).

Synchronous Rectification

Synchronous rectification improves efficiency by 3% to 5% at heavy loads when compared to a conventional Schottky rectifier. To prevent cross-conduction or "shoot-through," the synchronous rectifier turns on following a short delay (dead time) after the P-channel power MOSFET turns off. In discontinuous (light-load) mode, the synchronous rectifier switch turns off as the inductor current approaches zero. The synchronous rectifier works under all operating conditions, including Idle Mode.

Table 1. Output Voltage Selection

FBSEL PIN	AC LOAD REGULATION (%)	OUTPUT VOLTAGE (V)
IN	2	2.525
Unconnected	2	3.33
GND	1	Adjustable
V_{REF}	2	Adjustable

Integrator Amplifier (COMP)

An internal transconductance amplifier fine tunes the output DC accuracy. The transconductance amplifier is compensated at COMP. A capacitor from COMP to ground determines the gain-bandwidth product and the overall loop response. This integrator effectively eliminates any long-term error within the time constant set by the G_m of the transconductance amplifier and the capacitor connected to COMP.

For stability, choose COMP as follows:

$$C_{COMP} \geq \frac{G_m \times R_{LOAD} \times C_{OUT}}{4}$$

where G_m = 9.1µS.

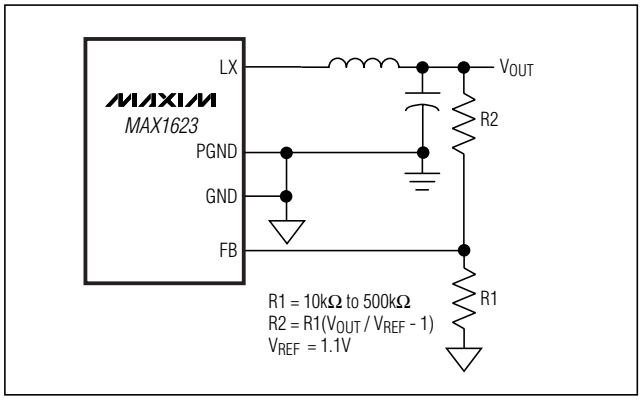


Figure 3. Adjustable Output Voltage

A high capacitor value maintains a constant average output voltage but slows the loop response to changes in output voltage. A low capacitor value speeds up the loop response to changes in output voltage. Choose the capacitor value that results in optimal performance.

Current Limiting

The current-sense circuit enables when the PMOS power switch is on. This circuit's corresponding output voltage feeds three separate comparators: the skip current comparator (1.25A), the maximum current comparator (4.15A), and the PWM current comparator (see the *Modes of Operation* section).

Oscillator Frequency and Programming the Off-Time

The MAX1623 features a programmable off-time that is set by R_{TOFF} connected from TOFF to GND. Connecting a 110kΩ resistor from TOFF to GND achieves a 1µs (nominal) off-time. The off-time is inversely proportional to R_{TOFF} according to the formula:

$$t_{OFF} = R_{TOFF} / 110k\ (\mu s)$$

t_{OFF} is adjustable between 0.5µs to 4µs (see the *Typical Operating Characteristics*). To set the switching frequency when the inductor operates in continuous-conduction mode, the off-time has to be set to:

$$t_{OFF} = \frac{V_I - V_O - V_{PCH}}{f\,(V_I - V_{PCH} + V_{NCH})}$$

where:

t_{OFF} = the programmed off-time

V_I = input voltage

V_O = output voltage

f = desired switching frequency during continuous inductor current

V_{PCH} = the voltage drop across the internal P-channel switch

V_{NCH} = the voltage drop across the internal N-channel synchronous rectifier

Switching frequency decreases as load current is decreased below the 625mA Idle Mode trip point.

Internal Reference

The 1.10V internal reference (available at REF) is accurate to ±1.5% over the -40°C to +85°C operating range, making it useful as a precision system reference. Bypass the reference to ground with a minimum 0.1µF ceramic capacitor. For low noise and jitter performance, use a 0.47µF ceramic capacitor. The reference can supply up to 10µA for external loads. However, if tight accuracy specifications for either reference or the main output are essential, avoid reference loads in excess of 5µA. Loading the reference reduces the main output voltage slightly, according to the reference-voltage load-regulation error.

Start-Up

To prevent the MAX1623 from false output regulation, the internal PMOS and NMOS switches will not switch on until all of the following conditions are true: the supply voltage is above the undervoltage lockout threshold, $\overline{SHDN}$ is pulled high, the internal reference voltage is at 75% of its nominal (1.1V) value, and the die temperature is below +145°C. When the above conditions are satisfied, the MAX1623 will regulate the output voltage to the selected level. The MAX1623 typically starts up in 1ms for full output load.

Thermal Shutdown and Overload Conditions

Thermal overload protection limits the MAX1623's total power dissipation. When the junction temperature reaches T_j = +145°C, the device turns off, allowing it to cool down. Switching resumes after the IC's junction temperature decreases by 20°C. If the thermal overload condition persists, the output pulses on and off.

Thermal overload protection is designed to protect the MAX1623 during fault conditions, such as an output short circuit.

Thermal Resistance

Junction to ambient thermal resistance (θ_{JA}) strongly depends on the amount of copper area immediately surrounding the IC's leads. The MAX1623 evaluation kit has 0.8in^2 of copper area. θ_{JA} on this board was measured to have 45°C/W of thermal resistance with no air

3A, Low-Voltage, Step-Down Regulator with Synchronous Rectification and Internal Switches

flow. A copper area of 0.4in^2 showed thermal resistance of 60°C/W.

Airflow over the IC can significantly reduce θ_{JA}.

Power Dissipation

The MAX1623's power dissipation consists mostly of conduction losses in the two internal power switches. Power dissipation due to supply current in the control section and average current used to charge and discharge the gate capacitance of the two power switches is less than 30mW at 300kHz. This number is reduced when switching frequency is reduced as the part enters Idle Mode.

Combined conduction loss in the two power switches is calculated by:

$$P_D = I_{LOAD}^2 (R_{ON})$$

where R_{ON} = 100mΩ (max).

The θ_{JA} required to deliver this amount of power is calculated by:

$$\theta_{JA} = (T_{J(MAX)} - T_{A(MAX)}) / P_D$$

where:

$T_{J(MAX)}$ = maximum allowed junction temperature

$T_{A(MAX)}$= maximum ambient temperature expected

Applications Information

Inductor L1

The inductor value can be adjusted to optimize the design for size, cost, and efficiency. Three key inductor parameters must be specified: inductance value (L), peak current (I_{PEAK}), and DC resistance (R_{DC}). The following equation includes a constant, denoted as LIR, which is the ratio of inductor peak-to-peak AC current to DC load current. A higher value of LIR allows smaller inductance, but results in higher losses and ripple. A good compromise between size and losses is found at a 30% ripple current to load current ratio (LIR = 0.3), which corresponds to a peak inductor current 1.15 times the DC load current:

$$L = \frac{V_{OUT}(V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \times f \times (I_{OUT})(LIR)}$$

where:

f = switching frequency

I_{OUT} = maximum DC load current

LIR = ratio of AC to DC inductor current, typically 0.3

Table 2. Suggested Values (V_{IN} = 5V, I_O = 3A, f = 300kHz)

V_{OUT} (V)	T_{OFF} (µs)	R_{TOFF} (kΩ)	L (µH)
3.3	1.10	120	4.7
2.5	1.67	180	4.7
1.8	2.16	240	4.7
1.5	2.38	260	3.9
1.1	2.68	280	3.3

The peak inductor current at full load is 1.15 x I_{OUT} if the above equation is used; otherwise, the peak current can be calculated by:

$$I_{PEAK} = I_{OUT} + \frac{V_{OUT}(V_{IN(MAX)} - V_{OUT})}{2 \times f \times L \times V_{IN(MAX)}}$$

The inductor's DC resistance is a key parameter for efficiency and must be minimized, preferably to less than 25mΩ at I_{OUT} = 3A. To reduce EMI, use a shielded inductor.

Input and Output Filter Capacitors (C1, C2)

Use a low-ESR input capacitor according to the input ripple-current requirements and voltage rating.

$$I_{RIPPLE} = I_{LOAD}\left(\sqrt{\frac{V_{OUT}\left(V_{IN} - V_{OUT}\right)}{V_{IN}}}\right)$$

In addition to C1, place a 10µF ceramic bypass capacitor from the power input (pin 2, 4, 6) to power ground (pin 15, 17, 19) within 5mm of the IC.

The output filter capacitor determines the output voltage ripple and output load-transient response, as well as the loop's stability.

The output ripple in continuous-conduction mode is:

$$V_{OUT(RPL)} = I_{OUT(MAX)} \times LIR\left(ESR_{C2} + \frac{1}{2\pi \times f \times C2}\right)$$

where f is the switching frequency.

Loop Stability

Stable operation requires the right output filter capacitor. When choosing the output capacitor, ensure the following conditions are met:

$$C_2 \geq 80 \times t_{OFF} \times \frac{V_{REF}}{V_{OUT}}$$

and

$$10m\Omega \leq R_{ESR}$$

Circuit Layout and Grounding

Good layout is necessary to achieve the intended output power level, high efficiency, and low noise. Good layout includes the use of a ground plane, appropriate component placement, and correct routing of traces using appropriate trace widths. For heatsinking purposes, copper area connected at the IC should be evenly distributed among the high-current pins.

1) Minimize high-current ground loops. Connect the input capacitor's ground, output capacitor's ground, and IC PGND together.
2) A ground plane is essential for optimum performance. In most applications, the circuit will be located on a multilayer board, and full use of the four or more copper layers is recommended. Use the top and bottom layers for interconnections and the inner layers for an uninterrupted ground plane.
3) Place the LX node components as close together as possible. This reduces resistive and switching losses and confines noise due to ground inductance.
4) Connect the input filter capacitor less than 10mm away from IN. The connecting copper trace carries large currents and must be at least 2mm wide, preferably 5mm.
5) Connect GND directly to PGND at only one point near the IC.

Chip Information

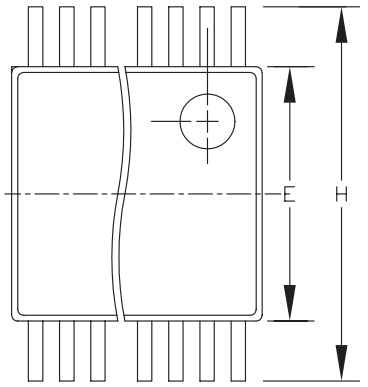
TRANSISTOR COUNT: 1220

3A, Low-Voltage, Step-Down Regulator with Synchronous Rectification and Internal Switches

Package Information

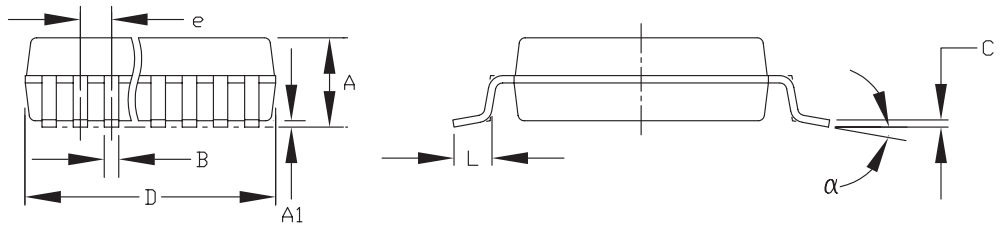
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

SSOP EPS



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.068	0.078	1.73	1.99
A1	0.002	0.008	0.05	0.21
B	0.010	0.015	0.25	0.38
C	0.004	0.008	0.09	0.20
D	SEE VARIATIONS			
E	0.205	0.209	5.20	5.38
e	0.0256 BSC		0.65 BSC	
H	0.301	0.311	7.65	7.90
L	0.025	0.037	0.63	0.95
α	0°	8°	0°	8°

	INCHES		MILLIMETERS		
	MIN	MAX	MIN	MAX	N
D	0.239	0.249	6.07	6.33	14L
D	0.239	0.249	6.07	6.33	16L
D	0.278	0.289	7.07	7.33	20L
D	0.317	0.328	8.07	8.33	24L
D	0.397	0.407	10.07	10.33	28L



NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO150.

MAXIM
PROPRIETARY INFORMATION
TITLE:
PACKAGE OUTLINE, SSOP, 5.3x.65mm

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0056	B	1/1

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